CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

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1. (Currently Amended) Apparatus comprising:

an array of computational cells coupled to one another and having a one-to-one correspondence with respective buffers of an array of buffers, wherein each computational cell includes:

a first input for receiving data corresponding to an availability status of the respective buffer corresponding to the computational cell;

a second input for receiving data corresponding to a currently selected buffer from among the array of buffers~~, the second input not for receiving the data from one of the array of computational cells~~; [[and]]

a first output upon which data is produced for identifying a next available buffer[[,]];

a third input; and

a second output coupled to the third input of a next computational cell, wherein the first output is coupled to logically AND the first input with the third input,

wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies a next buffer in the buffer array to be allocated.

2. (Currently Amended) The apparatus of Claim 1, wherein ~~each computational cell further comprises:~~

~~a third input; and~~

~~a second output coupled to the third input of a next computational cell,~~

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~~wherein~~ data is produced on the second output of a given computational cell as a function of data received at the first, second, and third inputs for the computational cell.

3. (Original) The apparatus of Claim 2, wherein each computational cell comprises:

an inverter for receiving data on the first input of the cell and having an output;

a first AND gate having a first input coupled to the output of the inverter; and a second input for receiving data on the third input of the cell, and having an output;

a second AND gate, having a first input for receiving data on the first input of the cell and a second input for receiving data on the third input of the cell, said second AND gate having an output corresponding to the first output of the cell; and

an OR gate, having a first input coupled to the output of the first and gate, and a second input for receiving the data on the second input of the cell, said OR gate having an output corresponding to the second output of the cell.

4. (Original) The apparatus of Claim 2, wherein the first input of a given computational cell is labeled A, the second input is labeled P, the third input is labeled I, the first output is labeled N, and the second output is labeled 0, and further wherein each computational cell produces a logic value at its first output N based on the logic equation,

$$N = A \text{ AND } I$$

and wherein each cell produces a logic value at its second output O based on the logic equation,

$$0 = P \text{ OR } (\text{NOT } A \text{ AND } I).$$

5. (Original) The apparatus of Claim 2, wherein a plurality of computational cells are arranged in a cascaded order so as to define 0^{th} to N^{th} computational cells such that the second output from an i^{th} computational cell is coupled to the third input of an $(i^{th} + 1)$

computational cell, and the second output from the N^{th} computational cell is coupled to the third input of the 0^{th} computational cell.

6. (Original) The apparatus of Claim 1, wherein the array of buffers comprises N buffers and data received at the first input of each computational cell collectively comprise an availability vector comprising N bits, each bit corresponding to an availability status of a respective buffer.

7. (Original) The apparatus of Claim 10, wherein the array of buffers comprises N buffers and data received at the second input of each computational cell collectively comprise a current selected entry vector comprising N bits, each bit corresponding to a respective buffer, said current selected entry vector including only one bit that is asserted, said asserted bit identifying a most recently allocated buffer.

8. (Original) The apparatus of Claim 1, wherein the array of buffers comprises N buffers and the next available buffer vector comprises N bits, each bit corresponding to a respective buffer, said next available buffer vector including only one bit that is asserted, said asserted bit identifying the next available buffer to be allocated.

9. (Currently Amended) A processor comprising:

an array of buffers;

an array of computational cells coupled to one another in a cascaded fashion, each computational cell corresponding to a respective buffer in the array of buffers and including:

a first input for receiving data corresponding to an availability status of a buffer corresponding to the computational cell;

a second input for receiving data corresponding to a currently selected buffer from among the array of buffers~~, the second input not for receiving the data from one of the array of computational cells~~;

a first output upon which data is produced for identifying a next available buffer,

a second output; and

a third input, coupled to the second output of a preceding computational cell,

wherein the first output is coupled to logically AND the first input with the third input, and wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies the next buffer in the buffer array to be allocated for use.

10. (Original) The processor of Claim 9, wherein said array of computational cells define 0^{th} to N^{th} computational cells, and the second output from the N^{th} computational cell is coupled to the third input of the 0^{th} computational cell.

11. (Previously Presented) The processor of Claim 9, wherein each computational cell comprises:

an inverter for receiving data on the first input of the cell and having an output;

a first AND gate having a first input coupled to the output of the inverter; and a second input for receiving data on the third input of the cell, and having an output;

a second AND gate, having a first input for receiving data on the first input of the cell and a second input for receiving data on the third input of the cell, said second AND gate having an output corresponding to the first output of the cell; and

an OR gate, having a first input coupled to the output of the first and gate, and a second input for receiving the data on the second input of the cell, said OR gate having an output corresponding to the second output of the cell.

12. (Original) The processor of Claim 9, wherein the first input of a given computational cell is labeled A, the second input is labeled P, the third input is labeled I, the first output is labeled N, and the second output is labeled 0, and further wherein each computational cell produces a logic value at its first output N based on the logic equation,

$$N = A \text{ AND } I$$

and wherein each cell produces a logic value at its second output O based on the logic equation,

$$0 = P \text{ OR } (\text{NOT } A \text{ AND } I).$$

13. (Previously Presented) A method comprising:

determining an availability vector corresponding to an availability status of each buffer in an array of buffers;

determining a current selected entry vector that identifies a most recently allocated buffer; and

determining a next available buffer vector that identifies the next available buffer to be allocated from among the plurality of buffers as a function of the availability vector and the current selected entry vector.

14. (Original) The method of Claim 13, wherein the array of buffers comprises N buffers and the availability vector comprises N bits, each bit corresponding to an availability status of a respective buffer.

15. (Original) The method of Claim 13, wherein the array of buffers comprises N buffers and the current selected entry vector comprises N bits, each bit corresponding to a respective buffer, said current selected entry vector including only one bit that is asserted, said asserted bit identifying a most recently allocated buffer.

16. (Original) The method of Claim 13, wherein the array of buffers comprises N buffers and the next available buffer vector comprises N bits, each bit corresponding to a respective buffer, said next available buffer vector including only one bit that is asserted, said asserted bit identifying a next available buffer to be allocated.

17. (New) The apparatus of claim 1, wherein the second input is not directly coupled to an adjacent one of the computational cells.

18. (New) The processor of claim 9, wherein the second input is not directly coupled to an adjacent one of the computational cells.